AMENDMENTS

In the Claims

This listing of claims replaces all prior versions and listings of claims in the application. Inserted language is underlined. Deleted language is denoted with a ~~strikethrough~~.

1. (currently amended): A method for forming a gate stack having improved electrical properties in a gate structure forming process comprising the steps of:

providing a semiconductor substrate;

forming a metal oxide layer over an exposed portion of the semiconductor substrate; and

forming a silicon-containing electrode layer over the metal oxide layer by depositing a silicon layer and introducing ~~in~~ a nitrogen containing ambient simultaneously.

2-4. (canceled)

5. (original): The method of claim 1, wherein the metal oxide layer comprises a dielectric constant of greater than about 20.

6. (original): The method of claim 1, wherein the metal oxide is formed having a thickness of about 20 Angstroms to about 100 Angstroms.

7. (original): The method of claim 1, wherein the gate stack including the metal oxide layer is formed to have a dielectric thickness equivalent to a silicon dioxide dielectric thickness of less than about 20 Angstroms.

8. (original): The method of claim 6, wherein the metal oxide is selected from the group consisting of tantalum oxides, titanium oxides, zirconium oxides, hafnium oxides, and yttrium oxides.

9. (original): The method of claim 8, wherein the metal oxide is formed from one of a metal-organic CVD method and an atomic layer deposition (ALD) method.

10. (original): The method of claim 9, wherein an ozone containing oxidation process is carried out to treat the metal oxide layer following the formation of the metal oxide layer.

11. (previously presented): The method of claim 1, wherein a layer comprising aluminum oxide is formed over the metal oxide layer.

12. (original): The method of claim 11, wherein the aluminum oxide layer is formed having a thickness of about 5 Angstroms to about 15 Angstroms.

13-32. (canceled)

33. (new): A method for forming a gate stack having improved electrical properties in a gate structure forming process comprising the steps of:

providing a semiconductor substrate;

forming a metal oxide layer over an exposed portion of the semiconductor substrate; and

depositing a polysilicon electrode over the metal oxide layer by a low pressure chemical vapor deposition (LPCVD) process simultaneously in association with a nitrogen containing ambient.

34. (new): The method of claim 33, wherein the LPCVD process comprises a cold-wall and a hot-wall configuration.